UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,693	10/29/2003	Michael Shur	SETI-0007	5258

23550 7590 09/28/2007

HOFFMAN WARNICK & D'ALESSANDRO, LLC
75 STATE STREET
14TH FLOOR
ALBANY, NY 12207

EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
09/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/696,693	SHUR ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,7,8,10,11,13-17,20,21,23-26,28 and 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7,8,10,11,13-17,20,21,23-26,28 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 05/14/2007 has been entered.

In view of the new grounds of rejection herein, this rejection is non-final.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claimed field effect transistor array and array of rectifying contacts (note claim 1) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Applicants' new or amended drawings (if such be required) must meet the following criteria:

> Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

It may be that "array of rectifying contacts" (as this term is used by the claims) simply means two or more rectifying contacts in proximity to each other, as suggested by existing figures 7 and 8 and language in the specification (paragraphs 0033-0035 – note that these paragraphs contain the only discussion of "arrays" found in the specification)

discussing the claimed "array of heterodimensional diodes." If such be the case, the claimed "array of rectifying contacts" is adequately represented by figures 7 and 8.

It may be (as the Examiner reasons below) that "field effect transistor array" (as this term is used by the claims) simply means placing two or more field effect channels in proximity to each other, as shown in figure 5. Such a construction of the term "field effect transistor array" is suggested by existing figures 7 and 8 and language in the specification (paragraphs 0033-0035 – note, again, that these paragraphs contain the only discussion of "arrays" found in the specification) discussing the claimed "array of heterodimensional diodes." If such be the case, the claimed "field effect transistor array" is adequately represented by figure 5.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by MALONEY (6,269,199).

Maloney discloses a method of generating radiation using a field effect transistor (note column 4 lines 21-23), the method comprising: shining a laser pulse (note column 7 lines 5-6) onto the field effect transistor; and adjusting a frequency of the radiation by adjusting a carrier density of carriers 230 (as shown in figure 3) in a channel (indicated 106 in figure 1; not numbered in figures 2-6) of the field effect transistor, wherein the adjusting uses a bias voltage (indicated as "SIGNAL" in figure 1, or V_{cc} in figure 6A) applied to a periodic grating gate (note column 6 lines 63-66) of the field effect transistor. Note figures 1, 3-5, 6A-B, column 4 lines 21-43, column 5 lines 58-68, column 6 lines 1-15 and 54-67, column 7 lines 1-13, and column 8 lines 6-18 of Maloney. Note that the carrier density of carriers adjusts (in the normal and usual course of operating the device) in response the step of imposing the bias voltage (indicated as "SIGNAL" in figure 1, or V_{cc} in figure 6A), as Maloney relates at column 4 lines 13-17. Applicants agree that the carrier density of carriers adjusts simply in response the step of imposing the bias voltage. Note paragraph 0028 of the instant application. Applicants further state that the frequency of the radiation adjusts simply in response to the change in carrier density. Note, again, paragraph 0028 of the instant application.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 7, 8, 13-17, 20, 21, 23-26 and 28 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Oda (5,371,388) in view of Brener et al. (5,729,017). New claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oda (5,371,388) in view of Brener et al. (5,729,017).

Regarding Claim 1, Oda discloses a semiconductor device where in Figs. 12 and 15, it is discloses a semiconductor device having a two dimensional carrier gas in the channel region (see claim 2 or Oda) comprises one of heterodimensional diode or field effect transistor, carrier gas excitation by laser light and adjusting the frequency of radiation using the voltage applied to the semiconducting device (see abstract section of Oda). Oda fails to disclose the duration of the laser light in order to have a terahertz radiation. However, Brener et al. disclose a terahertz generators and detectors where in' claim 3, a picoseconds/femtoseconds duration laser pulse applied to electrode in order to have a terahertz generation.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required duration for the laser pulse in Oda as taught by Brener et al. in order to have a semiconductor device with terahertz radiation.

Regarding Claim 2, Brener et al. disclose terahertz radiation.

Regarding Claim 3, abstract section of Oda discloses the adjustment of the gate voltage.

Regarding Claims 7 and 15, laser light is applied to top surface of Oda's device as shown in Fig. 12.

Regarding Claims 8, 13 and 14, in Fig. 12 of Oda, laser light is applied to gate/source spacing and in Fig. 15; the laser light is applied to the gate.

Regarding Claim 10, in Fig. 12 Oda discloses an indium-tin-oxide transparent gate. Note figure 12 and column 9 lines 5-8.

Regarding Claim 17, Fig. 12 of Oda discloses the first and the second laser lights.

Regarding Claim 20, Figs. 1 and 7 of Brener et al. disclose the contact structure.

Regarding Claim 21, claim 2 of Oda discloses the two-dimensional carrier gas.

Regarding Claims 23 and 25, Brener et al. disclose the required picoseconds duration laser pulse in claim 3.

Regarding Claims 26 and 28, Brener et al. disclose the terahertz semiconductor device.

Regarding Claim 29, Oda discloses an active layer 30 in the field effect transistor. Further, as discussed above, Oda discloses the step of shining laser light ($h\nu$) onto said active layer. Note figure 12 of Oda. As Applicants point out at paragraph 0027 of their application, in its normal and usual operation, the result of shining laser light on an active layer such as Oda's layer 30 would be to excite plasma oscillations and trap them as plasma waves.

Response to Arguments

5. Applicant's arguments filed 05/14/2007 have been fully considered but they are not persuasive.

It is argued, at pages 8-9 of the remarks, that "Applicants respectfully submit that the device in Oda is not a heterodimensional diode." Applicants' submission begs the question of just what the heck (within the meaning assigned to this term by the claims) a "heterodimensional diode" is.

During patent examination, the pending claims must be given their "broadest reasonable interpretation consistent with the specification." In re Hyatt, 21 1 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). While the claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allow.

In re American Academy of Science Tech Center, WL 1067528 (Fed. Cir. May 13, 2004) (The USPTO uses a different standard for construing claims than that used by district courts; during examination the USPTO must give claims their broadest reasonable interpretation). This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989); Chef America, Inc. v. Lamb-Weston, Inc., 358 F.3d 1371, 1372, 69 USPQ2d 1857 (Fed. Cir. 2004).

Heterodimensional (HD) devices are defined as "devices based on contacts of dissimilar dimensions." Note page 42 and figure 1 of Nabet et al., "Heterojunction and heterodimensional devices for optoelectronics." A "diode" is defined as a p-n junction in a semiconductor wafer. Note page 257 and figure 5.15 of Muller and Kamins, "Device Electronics for Integrated Circuits." The "plain meaning" of "heterodimensional diode" is thus a contact of dissimilar dimensions forming a p-n junction in a semiconductor wafer. Oda's device prominently features such two such contacts, where three-dimensional n^+-diffused regions 36 and 37 contact p-type two dimensional electron gas 30. Note figure 12, column 8 lines 61-68, and column 13 lines 15-19 of Oda.

Note that the elements must be arranged (as Oda arranges the elements of his "heterodimensional diode") as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d

1566 (Fed. Cir. 1990). See MPEP § 2131. Applicants are three of a small group[1] of individuals who have been trying for about eight years now to get the mainstream semiconductor industry to recognize the term "heterodimensional" for the commonplace circumstance of a contact[2] between charge carrying regions of dissimilar dimensions. The fact that the mainstream semiconductor industry (including Oda and Brener et al.) has stubbornly resisted efforts to popularize the term "heterodimensional" seems inapposite as a reason for allowing Applicants' claims. Note that in the over eight million patents and patent publications in the USPTO database, the term "heterodimensional" is used exactly twice. One such use is the publication of the present application. The other is a publication of an application by Cheng, Greer, Kennedy, and Mathewson, four more of the individuals named below in footnote 1. Like the present applicants, Cheng, Greer, Kennedy, and Mathewson used the term "heterodimensional" with the blithe assumption that the rest of us actually knew (without having it explained to us) what

---

[1] Aniel, F.; Anwar, A.; Brown, E.R.; Castro, F.; Cataldo, A.; Cheng, T; Chu, J.O.; Cola, A.; Crowe, T.W.; Danneville, F.; Deen, M.J.; Deng, J.; Ekuakille, A.L.; Fareed, R. S. Q.; Fjeldly, T.A.; Gaska, R.; Gonzales, J.; Greer, J.C.; Grimm, W.J.; Hamid, H.A.; Hornsey, R.I.; Hu, X.; Hurt, M.J.; Hyunchang Park; Iniguez, B.; Jian-Qiang Lu; Jimenez, D.; Jung-Hui Tsai; Kelly, M.J.; Kennedy, M.P.; Knights, A.P.; Koester, S.J.; Koh, P.J.; Lazaro, A.; Lu, J. -Q.; Maki, P.; Manzoli, J.; Marsal, L.F.; Mathewson, A.; Meneghesso, G.; Moon, B.J.; Nabet, B.; Nazimudeen, A.S.; Pala, N.; Pallares, J.; Park, H.; Peatman, W.C.B.; Quaranta, F.; Rabkin, P.B.; Ragi, R.; Roig, J.; Romero, M.A.; Romisch, S.; Rooks, M.J.; Rumyantsev, S.; Ryzhii, V.; Schuermeyer, F.; Shur, M.S.; Tait, G.B.; Tongwei Cheng; Trotta, A.; Tsai, R.; Veksler, D.; Webster, C.S.; Weiss, M.D.; Ying Huang; Ytterdal, T.; Yu-Chi Kang; and Zanoni, E,, by the Examiner's count.

[2] Note that if contact between charge carrying regions of dissimilar dimensions were not possible, those of us who live in the three dimensional world (which might even include some Applicants' "heterodimensional" colleagues) would not be able to take advantage of two-dimensional currents such as the ones generated internal to Oda's device. Note that Oda disclosed this device in 1994, well before Nabet, Shur, Peatman, Gaska, Castro, and colleagues began the current effort to popularize "heterodimensional" as a term of art.

"heterodimensional" meant. Another Examiner (who simply assumed that "heterodimensional" meant "incorporating a heterojunction") rejected their case, and it went abandoned.

It is argued, at page 9 of the remarks, that "With further respect to claim 1, Applicants respectfully submit that the Office fails, inter alia, to show that Oda teaches adjusting a frequency of the radiation using a voltage applied to the semiconducting device as in claim 1. In support of its rejection, the Office cites the Abstract of Oda as allegedly teaching this feature. Office Action, p. 2. However, Applicants note that Oda's Abstract does not include any discussion of adjusting a frequency of radiation, let alone doing so using a voltage applied to the semiconducting device as in claim 1."

In the Examiner's view, Applicants are confusing a step (applying a voltage to the semiconducting device) that may be performed by a device under the control of an individual, with the result (radiation has its frequency adjusted) achieved by the performance of said step. In a device (such as Oda's) of the sort used to perform the claimed method, characteristics of the two-dimensional carrier gas, once modified by adjusting the applied voltage, inevitably adjust the frequency of the radiation generated by the device. This fact, as far as Applicants are concerned, is indisputable. Note the last sentence of paragraph 0007 of Applicants' specification ("Characteristics of the two-dimensional carrier gas are modified by adjusting the applied voltage, which in turn adjusts the frequency of the radiation generated by the device"), and paragraph 0028 of

Applicants' specification ("[T]he frequency of the plasma waves is also proportional to the square root of a carrier density in the active layer 16 (i.e., channel)... since the carrier density can be adjusted by applying a voltage to device 10, the frequency of the plasma waves is also approximately proportional to the square root of the voltage difference between a threshold voltage and a voltage applied to gate 20. In other words, changing the bias voltage at gate 20 and/or the length of gate 20 adjusts the frequency of the plasma waves which also adjusts the frequency of the radiation").

Under the principles of inherency, if a prior art device, in its normal and usual operation, would necessarily perform the method claimed, then the method claimed will be considered to be anticipated by the prior art device. When the prior art device is the same as a device described in the specification for carrying out the claimed method, it can be assumed the device will inherently perform the claimed process. *In re King,* 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986). This is the case here. Oda and Brener et al. suggest a device identical to the device Applicants describe in their specification as capable of performing the claimed process. Oda and Brener et al. suggest applying a voltage to said device. It is specious for Applicants to protest that such a device could never have produced a particular natural (note that Applicants themselves state that the frequency of the plasma waves is proportional to the square root of a carrier density in the active layer) result until subjected to Applicants' control. See MPEP § 2112.02.

Applicants write, "Should the Office maintain this interpretation of Oda, Applicants respectfully request that the Office clarify how Oda allegedly teaches adjusting a frequency of the radiation using a voltage applied to the semiconducting device." However, *King* held

> Here, appellant's burden before the board was to prove that Donley's structure does not perform the so-called method defined in the claims when placed in ambient light. Appellant did not satisfy that burden. It did not suffice merely to assert that Donley does not inherently achieve enhanced color through interference effects, challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks. See *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972), quoted with approval in *In re Fitzgerald*; *In re Best*, supra.

King, 801 F.2d at 1331, 231 USPQ at 139. According to this holding, it is the Examiner who should respectfully request Applicants to clarify why it should be that Oda's application of a voltage to a device that is apparently identical to the one Applicants apply their voltage to can produce a different result from the result Applicants report (and claim). See MPEP § 2112. See also *In re Best,* 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977). The *Best* applicant claimed a process for preparing a hydrolytically stable zeolitic aluminosilicate which included a step of "cooling the steam zeolite ... at a rate sufficiently rapid that the cooled zeolite exhibits a X-ray diffraction pattern...." A U.S. patent to Hansford expressly disclosed all the process limitations except the cooling step. The court stated that any sample of Hansford's zeolite would necessarily be cooled to facilitate subsequent handling. Therefore, a *prima facie* case under 35 U.S.C. 102/103 was made. Applicant had failed to introduce any evidence comparing X-ray diffraction patterns showing a difference in cooling rate between the

claimed process and that of Hansford or any data showing that the process of Hansford would result in a product with a different X-ray diffraction. Either type of evidence would have rebutted the *prima facie* case.

Applicant is asked to please keep in mind that "[T]he PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his [or her] claimed product. Whether the rejection is based on 'inherency' under 35 U.S.C. 102, on '*prima facie* obviousness' under 35 U.S.C. 103, jointly or alternatively, the burden of proof is the same...[footnote omitted]." The burden of proof is similar to that required with respect to product-by-process claims. *In re Fitzgerald,* 619 F.2d 67, 70, 205 USPQ 594, 596 (CCPA 1980) (quoting *In re Best,* cited above). It will not suffice merely to assert that Oda does not inherently achieve adjusting a frequency of the radiation (as King asserted Donley did not inherently achieve enhanced color through interference effects), challenging the PTO to prove the contrary by experiment or otherwise. "The PTO is not equipped to perform such tasks." *King,* 801 F.2d at 1331, 231 USPQ at 139.

It is argued, at page 10 of the remarks, that "With respect to claim 8... the Office fails, inter alia, to show that Oda or Brener teaches or suggests adjusting a frequency of the radiation by adjusting a carrier density of carriers in a channel of the field effect transistor, wherein the adjusting includes adjusting a gate length for the gate as in claim 8. Applicants note that neither Oda nor Brener includes any discussion related to the

adjusting in claim 8. Further, the Office does not address this feature in the Office Action."

However, "adjusting a gate length," in the context of Applicants' claims, means nothing more or less than the process of setting aside a device having a particular gate length and picking up a different device that happens to have a different gate length. Note paragraph 0030 and figure 4 of the application as filed. The device disclosed in Oda may come in a variety of gate lengths.

Applicants write, "[S]hould the Office maintain this rejection, Applicants respectfully request that the Office particularly point out how Oda or Brener allegedly teaches or suggests adjusting a frequency of the radiation by adjusting a carrier density of carriers in a channel of the field effect transistor, wherein the adjusting includes adjusting a gate length for the gate as in claim 8." The Examiner's answer is the same: It is Applicant's duty, not the Examiner's, to demonstrate how apparently identical devices can produce different results under the same stimulus. *King,* 801 F.2d at 1331, 231 USPQ at 139; *Fitzgerald,* 619 F.2d at 70, 205 USPQ at 596; *Best,* 562 F.2d at 1255, 195 USPQ at 433. Applicants are respectfully requested to clarify how the results of comparing a series of the devices Oda discloses, each having a different gate length, could differ from the results of comparing a series of identical devices (as Applicants do, note figure 4 of the application) to obtain the results Applicants report (and claim).

It is further argued at page 10 that "With respect to claim 10... the Office fails, inter alia, to show that Oda or Brener teaches or suggests adjusting a frequency of the radiation by adjusting a carrier density of carriers in a channel of the field effect transistor, wherein the field effect transistor comprises a transparent gate, and wherein the laser pulse is shone onto the transparent gate as in claim 10. Applicants note that neither Oda nor Brener includes any discussion related to the adjusting in claim 10. Further, the Office does not address this feature in the Office Action." Applicants next argue, at page 11, that "With respect to claim 11, Applicants respectfully submit that the Office fails to establish a prima facie case of obviousness. For example, the Office fails, inter alia, to show that Oda or Brener teaches or suggests adjusting a frequency of the radiation by adjusting a carrier density of carriers in a channel of the field effect transistor, wherein the adjusting uses a bias voltage applied to a periodic grating gate of the field effect transistor as in claim 11. Applicants note that neither Oda nor Brener includes any discussion related to the adjusting in claim 11."

These arguments, while superficially similar to the Applicants' arguments concerning claims 1 and 8, assert that neither Oda nor Brener teaches or suggests the use of a transparent or periodic grating gate.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of

that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). See MPEP § 2143.03.

Oda in fact teaches a transparent gate. Oda's second embodiment, note figure 12 and column 9 lines 5-8, utilizes a transparent indium-tin-oxide (ITO) Schottky gate. The previous action simply neglected to point this fact out. The action states, page 3 line 7, "Regarding Claims 10 and 11, Oda discloses a field effect transistor in claim 1," and then stops abruptly. One may speculate that the writer intended to add more, but for some reason neglected this point. Perhaps the writer was distracted by a need to search Oda for the periodic gate of claim 11, a search that would have proven fruitless.

With regard to claim 11's periodic grating gate, Applicant's argument has merit. Neither Oda nor Brener teaches or suggests the use of such a gate. Applicants' argument with regard to claim 11 is therefore persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, new grounds of rejection are made in view of Maloney 6,269,199.

It is further argued at page 11 that "With respect to claims 13 and 14... the Office fails, inter alia, to show that Oda or Brener teaches or suggests adjusting a frequency of radiation by adjusting a carrier density of carriers in a channel of a field effect transistor as in claims 13 and 14. Applicants note that neither Oda nor Brener includes any discussion related to the adjusting in claims 13 and 14. Further, the Office does not address this feature in the Office Action." Applicants continue, "Applicants respectfully

request that the Office particularly point out how Oda or Brener allegedly teaches or suggests adjusting a frequency of radiation by adjusting a carrier density of carriers in a channel of a field effect transistor as in claims 13 and 14."

In point of fact there is no easier task than pointing out how adjusting a carrier density of carriers (as Oda does by changing the voltage on an adjacent gate) in a channel of a field effect transistor naturally and inherently results in adjusting a frequency of radiation.

"Characteristics of the two-dimensional carrier gas are modified by adjusting the applied voltage, which in turn adjusts the frequency of the radiation generated by the device." Application at paragraph 0007. "[T]he frequency of the plasma waves is also proportional to the square root of a carrier density in the active layer 16 (i.e., channel)... since the carrier density can be adjusted by applying a voltage to device 10, the frequency of the plasma waves is also approximately proportional to the square root of the voltage difference between a threshold voltage and a voltage applied to gate 20. In other words, changing the bias voltage at gate 20 and/or the length of gate 20 adjusts the frequency of the plasma waves which also adjusts the frequency of the radiation." Application at paragraph 0028. It is thus clear that adjusting a carrier density of carriers (as Oda does by changing the voltage on an adjacent gate) in a channel of a field effect transistor results (without further intervention) in adjusting a frequency of radiation.

It is argued, at page 12 of the remarks, that "With respect to claim 15... the Office fails, inter alia, to show that Oda or Brener teaches or suggests ... using a voltage applied to a heterodimensional diode to adjust a frequency of a plasma wave in a two-dimensional carrier gas in the heterodimensional diode as in claim 15. Applicants note that neither Oda nor Brener includes any discussion related to the adjusting in claim 15. Further, the Office does not address this feature in the Office Action." However, as explained above, "[T]he frequency of the plasma waves is ... proportional to the square root of a carrier density in the active layer" (i.e., channel). Application at paragraph 0028. Because "the carrier density can be adjusted by applying a voltage," (id.) "the frequency of the plasma waves is also approximately proportional to the square root of the voltage difference between a threshold voltage and a voltage applied to [a] gate." In other words, "changing the bias voltage at [a] gate ... adjusts the frequency of the plasma waves." Applicants do not dispute that Oda teaches applying a voltage to the device. Applicants specifically admit (paragraph 0028) that the natural result of applying this voltage is to adjust the carrier density. Applicants further admit (paragraph 0028) that the frequency of the plasma waves will (by the force of natural law) be proportional to the square root of the adjusted carrier density.

It is further argued at page 12 that "With respect to claims 21 and 28... the Office fails, inter alia, to show that Oda or Brener teaches or suggests providing a field effect transistor having a periodic grating gate as in claims 21 and 28. Applicants note that

neither Oda nor Brener includes any discussion related to a field effect transistor having a periodic grating gate as in claims 21 and 28. Further, the Office does not address this feature in the Office Action."

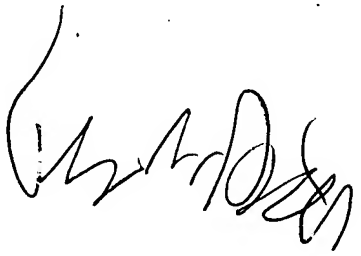
In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a step of a field effect transistor having a periodic grating gate) are not recited in claims 21 and 28. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



/Thomas L. Dickey/
Primary Examiner
Art Unit 2826